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Project Number: 101119624

Acronym: OWIN6G

Project title: Optical and Wireless Sensors Networks for 6G Scenarios

Work Package 3: Network Layer

Deliverable D3.1 (D31): Report on activities of Task 3.1

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Executive Summary

In this report, the progress on Task 3.1 for the work package 3 is presented.

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1. Work Package 3 Objectives

The WP3 objectives are shown in Table 1. Highlighted in bold are the items covered in this report that are related to T3.1 activities.

Table 1 WP3 main objectives

#i	WP3 Objectives
1.	Develop **functional and non-functional requirements** for a range of OWIN6G application scenarios;
2.	Investigating Software Defined Networking (SDN)-based management for OWIN6G with adoptability and enhanced security as well as creating an appropriate platform;
3.	Provide an optimization framework for hybrid OWC/RF architectures;
4.	Develop the project's pilots to be used as experimental demos as part of doctoral candidates' (DCs) research projects.

2. General Progress

Due to the different recruitments and the start timelines of DCs involved in WP3, the expected progress is in at the early stages. However, this is an initial report on how to organize, report and summarize the progress of WP3. Note that the tasks, deliverables, and milestones are outlined in the OWIN6G webpage [OWI].

3. Specific Progress Made

- Task 3.1 includes Network hardware definition with regard to OWIN6G application scenarios.
- Task lead: UV and all beneficiaries are involved. The task duration is 2 months (M7-M8).
- What is being achieved: Only data for DCs that were enrolled and active during M7&8 are presented, which includes the following:
  - (i) Consultation with partners involved with WP1 and WP2.
  - (ii) Consultation on initial application scenarios for OWIN6G.
  - (iii) Report on the development boards and embedded systems.

Those results are summarised in the following section.

3.1 Specific outcomes from T3.1

Two main questions on T3.1 were asked from beneficiaries on their involvement in WP1 and WP2 and how it will be linked to WP3. The following summarises their responses.

Q1. Outline the hardware definition of the embedded system from MAC layer definitions (WP2) and initial definitions of hardware implementation (WP1).

A. **Important definitions from WP1 (source: beneficiary)**

1) Communication technology to be used as an interface of data retrieved from the physical layer.

   a) An optical/electrical converter is required to convert the received optical sensing signals into analysable electrical signals (EPL)

2) Data format to be retrieved from physical platforms.

   a) Optical signal defined in terms of wavelength and intensity (EPL)

   b) Use of sensors for environmental monitoring such as air quality sensors for detecting the percentage of different gases and compounds, localization sensors and sensors used in healthcare for patient monitoring (IT).

3) Figure of merit that you are looking for to assure functionality of the expected sensors and WSN platform.

   a) Fabrication of fibre Bragg grating (FBG) sensor and optical interferometer-based sensor. Characterization of fabricated sensors to assure their functionality, i.e., sensor sensitivity, e.g., 10 ppb for ammonia, and 10 pg/ml for biomarker (EPL).

4) Requirements that the interface with MAC and network should be accomplished to assure the deployment of your sensor.

   a) Optical/electrical conversion module (EPL).

   b) Optical camera communications (OCC) will be used for capturing data from sensors (IT).

B. **<u>Important definitions from WP2 (source: beneficiary)</u>**

1) Communication technologies to be used as an interface of data retrieved from the physical layer and MAC layer.

   a) Optical/electrical converter (EPL).

   b) Free space optics (FSO)/visible light communication (VLC)/OCC for back-haul links (CTU, IT).

   c) Wi-Fi/Bluetooth/ZigBee for sensor nodes connectivity (CTU).

   d) A specific application of infrared optical wireless communication (OWC), namely wireless body area networks (WBANs) (ECM).

   e) Simulation of a hybrid VLC (downlink) – IR (uplink) system. The focus will be on optimizing parameters related to the PHY layer to maximize the battery life of the sensor nodes (HUA).

2) Data format to be retrieved and used under the MAC layer.

   a) Optical signal defined in terms of wavelength and optical intensity (EPL).

   b) An image sensor for capturing the sensor nodes for processing and decoding using the Raspberry Pi (IT, NU).

   c) The access point serves as a controller / DB controller for storing and relaying the real-time sensor data (CTU).

   d) Millimetre wave transmission as part of a hybrid communication link for sensing applications (CTU).

3) MAC protocols and their network requirements from WP2.

   a) The MAC protocol should manage low power consumption (even weeks or months of battery life), scalability, and low latency for WBANs. (ECM)

4) Figure of merit used and constraints.

    a) Sensor sensitivity (EPL).

    b) Optical receiver sensitivity (IT, NU).

5) Findings on energy efficiency if there are any related from WP2.

    a) Development of a simulation framework for OWC networks and the utilization of optimization algorithms to maximize energy efficiency (HUA).

    b) An optical sensor is a passive device and therefore no need for power. However, the laser source and the optical spectrum analyser will need power (EPL).

    c) IEEE MAC protocols revealed that the IEEE 802.15.7 MAC protocol exhibits greater energy efficiency compared to its counterpart, IEEE 802.15.6 (ECM).

Q2. Practical uses of development boards for WP3.

A. **Development boards and embedded systems (UV)**

1) **Arduino Uno Platform** - For generating ASCII identifiers, modulated using Manchester coding. By implementing this technique, the aim is to achieve positioning using visible light communication (VLC) while operating at low data rates.

2) **Raspberry Pi -** Sending separate bit identifiers, also codified in Manchester, to explore visible light positioning techniques and evaluate key performance parameters of positioning accuracy and the bit error rate (BER) as a function of signal-to-noise ratio (SNR).

3) **Pynq Z2 -** The Pynq Z2 uses Xilinx Zynq-7000 SoC, which combines the processing power of dual ARM Cortex-A9 cores (32 bits) with the flexibility and reconfigurability of FPGA fabric. This SoC architecture enables seamless integration of software and hardware components, allowing developers to implement complex embedded systems with both processing and programmable logic capabilities on a single chip. Its FPGA capabilities opened avenues for applications in signal processing, communication protocols, and real-time data processing, particularly in scenarios involving optical and RF communications.

    a) **ML-Based Security**: The board's computational capabilities, including the ARM cores and FPGA fabric, enable the implementation of ML-based security algorithms for anomaly detection, intrusion detection, and threat mitigation at the physical layer. Image processing based on ANN is available on this platform and will be evaluated under ML approaches such as RL.

    b) **Algorithm Implementation**: Leveraging the FPGA capabilities to implement custom encryption, authentication, and key exchange algorithms directly in hardware, enhancing the security of communication protocols and data transmission.

    c) **Sensing and Monitoring**: The Pynq Z2 can interface with sensors and monitoring devices via its GPIO, PMOD, and other interfaces. These sensors can be utilized for detecting physical intrusions, environmental anomalies, or unauthorized access, enhancing the security posture of embedded systems deployed on the board.

    d) **Peripheral Interfaces**: The Zynq-7000 SoC integrates a wide range of peripheral interfaces, including Ethernet, USB, HDMI, GPIO, SPI, I2C, UART, and more. These interfaces enable connectivity with external devices, sensors, displays, and networks, facilitating data exchange, communication, and interaction in embedded systems.

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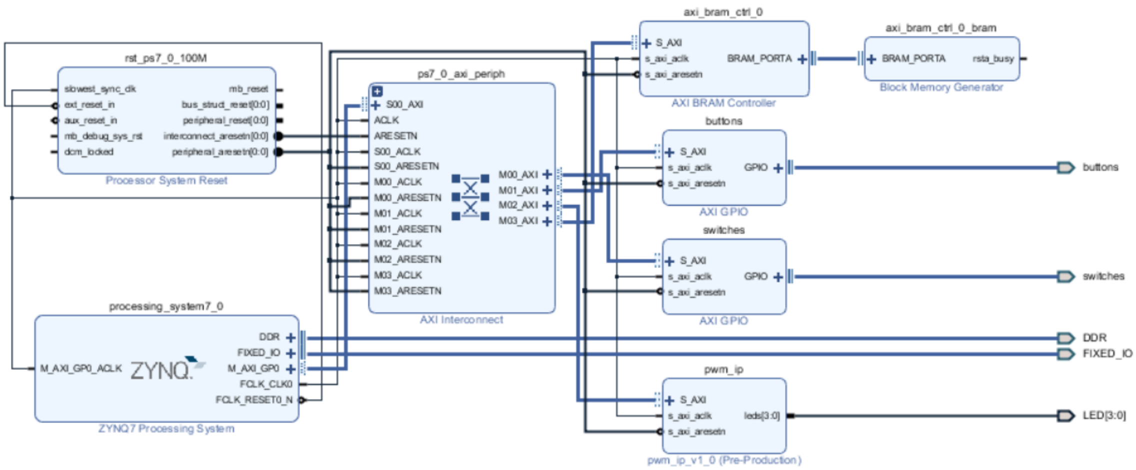

- Figure 1: **Pynq Z2 –** PWM generation block design in VIVADO.

3.2 List of publications

No publications related to T3.1 were submitted at the time of this deliverable.

4. Summary

The report outlined the first technical deliverable of OWIN6G related to the beneficiaries' requirements (software/hardware) for WP1 and WP3 regarding the network layer.

5. Future works

T3.1 is the initial snapshot and trial of how the project has progressed since the first DCs enrolments. During the following months, more outcomes and milestones will be completed as part of the project. Further works on security and network layer implementations will be carried out in collaboration with other DCs.

6. References

[OWI] OWIN6G web page. www.owin6g.eu . Last accessed by 15/05/24

Annex A. ACRONYMS

CTU	Czech technical university
IT	Instituto de Telecomunicações
EPL	Eblana Photonics
ECM	Ecole Central Méditerranée
UV	Universitat de Valencia
HUA	Harokopio University
PWM	Pulse width modulation
OWC	Optical wireless communications
FPGA	Field programmable gate array
VLC	Visible light communication
IR	Infrared
FBG	Fibre Bragg grating
WSN	Wireless Sensor Network
DB	Database
WPi	Work Package i
Ti.i	Task i.i
Di.i	Deliverable i.i